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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,044	06/09/2000	Christopher J. Duguay	SYNER-164XX	2567

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EXAMINER
SERRAO, RANODHI N

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/591,044	Applicant(s) DUGUAY ET AL.
	Examiner Ranodhi Serrao	Art Unit 2181

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 June 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

comprises an SMBus (Specification, column 1, lines 31- 40). Trieu et al. does not teach operative at least at the second clock rate to store at least a portion of the data in a register; and operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device. Carson et al. teaches operative at least at the second clock rate to store at least a portion of the data in a register (Specification, column 5, line 61 – column 6, line 6); and operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device (Specification, column 8, lines 9-13). At the time the invention was made, it would be obvious to a person of ordinary skill in the art to include operative at least at the second clock rate to store at least a portion of the data in a register; and operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device as taught by Carson et al. in the method of Trieu et al. because the data needs to be stored, and it is efficient to store it in a register.

3. As per claim 2, Carson et al. disclose the claimed invention as described above in claim 1. Furthermore, Carson et al. teaches the first device is further operative at least at the second clock rate to clear the data from the register upon completion of a data transfer (Specification, column 8, lines 15-17).

4. As per claim 6, Carson et al. disclose the claimed invention as described above in claims 1 and 2. Furthermore, Carson et al. teaches the method comprising the steps of: while the clock signal is being transmitted at least at the second clock rate, storing at least a portion of the data in a register communicably coupled to the bus (Specification, column 5, line 61 – column 6, line 6); and driving the clock line to a low logic level while the data is stored in the register (Specification, column 8, lines 9-13).

5. As per claim 7, Carson et al. disclose the claimed invention as described above in claims 1, 2, and 6. Furthermore, Carson et al. teaches including the step of clearing the data from the register upon completion of a data transfer (Specification, column 8, lines 15-17).

6. Claims 3, 4, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trieu et al. in view of Carson et al. as applied to claims 1 and 6 above, and further in view of Hamilton et al. (4,443,845).

7. As per claim 3, Trieu et al. in view of Carson et al. teaches a system for transferring data between a plurality of devices communicably coupled to a bus, the bus including at least one data line for transmitting the data and at least one clock line, the system comprising: the system being operative at a first clock rate and at a second clock rate less than the first clock rate; a first device communicably coupled to the bus and operative at least at the second clock rate to store at least a portion of the data in a register; and a second device communicably coupled to the bus and operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device. Trieu et al. in view of Carson et al. does not teach including pull-up circuitry for pulling the clock line to a high logic level, and wherein the second device is further operative to release the clock line upon completion of a data transfer to allow the clock line to be pulled-high by the pull-up circuitry. Hamilton et al. teaches including pull-up circuitry for pulling the clock line to a high logic level (Specification, column 50, lines 62-68); and wherein the second device is further operative to release the clock line upon completion of a data transfer to allow the clock line to be pulled-high by the pull-up circuitry (Specification, column 51, line 38 – column 52, line 4). At the time the invention was made, it would be obvious to a person of ordinary skill in the art to include including pull-up circuitry for pulling the clock

line to a high logic level, and wherein the second device is further operative to release the clock line upon completion of a data transfer to allow the clock line to be pulled-high by the pull-up circuitry as taught by Hamilton et al. in the method of Trieu et al. in view of Carson et al. because releasing the clock line allows devices to use it for other purposes.

8. As per claim 4, Hamilton et al. disclose the claimed invention as described above in claim 3. Furthermore, Hamilton et al. teaches including pull-up circuitry for pulling the clock line to a high logic level (Specification, column 50, lines 62-68); and wherein, upon completion of a data transfer, the first device is further operative to clear the data from the register (Specification, column 8, line 57 – column 9, line 22); and the second device is further operative to release the clock line to allow the clock line to be pulled high by the pull-up circuitry (Specification, column 51, line 38 – column 52, line 4).

9. As per claim 8, Hamilton et al. disclose the claimed invention as described above in claims 3 and 4. Furthermore, Hamilton et al. teaches the clock line is pulled to a high logic level by pull-up circuitry (Specification, column 50, lines 62-58); and further including the step of releasing the clock line upon completion of a data transfer to allow the clock line to be pulled-high by the pull-up circuitry (Specification, column 51, line 38 – column 52, line 4).

10. As per claim 9, Hamilton et al. disclose the claimed invention as described above in claims 3, 4, and 8. Furthermore, Hamilton et al. teaches the clock line is pulled to a high logic level by pull-up circuitry (Specification, column 50, lines 62-68); and further including the steps of, upon completion of a data transfer, clearing the data from the register (Specification, column 8, line 57 – column 9, line 22); and releasing the clock line to allow the clock line to be pulled-high by the pull-up circuitry (Specification, column 51, line 38 – column 52, line 4).

DETAILED ACTION

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 2, 5, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trieu et al. (5,925,135) in view of Carson et al. (5,920,156).

2. As per claims 1 and 5, Trieu et al. teaches a system for transferring data between a plurality of devices communicably coupled to a bus (Specification, column 1, lines 23-30); the bus including at least one data line for transmitting the data and at least one clock line, the system comprising (Specification, column 1, lines 52-65): the system being operative at a first clock rate and at a second clock rate less than the first clock rate (Abstract); a first device communicably coupled to the bus (Specification, column 1, line 66 – column 2, line 1); and a second device communicably coupled to the bus (Specification, column 2, lines 2-9). The bus

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hudson et al. (6,173,350) teaches a system and method for writing data to a serial bus from a smart battery.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ranodhi Serrao whose telephone number is (703) 305-8071. The examiner can normally be reached on M-F; 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Wong can be reached on (703) 305-3477. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

RNS
September 10, 2002

PETER WONG
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100